MONITORING IC PROCESS PARAMETERS WITH STATISTICALLY ENHANCED TEST PATTERN DATA

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ABSTRACT

Standard practice, among manufacturers of large scale integrated circuits, is the emplacement of test patterns on wafers. These test patterns are generally transistors in some simple circuit configuration. The role of such test patterns is to ascertain whether salient process control parameters are satisfied during the manufacture of a wafer. That is, tests, which determine quantities as threshold voltage, resistivity, etc. are performed on the patterns. Should the results of the tests not fall within certain acceptance ranges, it is assumed to be economically unfeasible to further process the wafer.

A questionable assumption in this procedure is that the measurements, made at the location of the test patterns, is absolutely indicative of the process control parameters for the remainder of the wafer. One anticipates that a probabilistic validity of this assumption will vary inversely with the geometric distance between a test pattern and an integrated circuit chip.

It is possible to develop an algorithm, based on a collection of statistical data, which remedies the uniformity assumption of process control parameter measurements. By gathering mean and variance data of the process parameters for the production runs, one can statistically relate process parameter variation on the wafers. One collects individual parameter distributions for each production run and composite distributions summarizing all of the runs.

Assume that the acceptance ranges for the parameters have been defined. By utilizing measurements of test patterns that are already present on production wafers, Bayesian analysis can be performed on the aforementioned statistical data. Consequently, a parameter distribution can be obtained which incorporates both the parameter measurements usually available and statistical information reflecting parameter non-uniformity. The above approach together with the acceptance range for the parameter and a percentile confidence enables a confidence interval to be established for the production wafer test pattern data. Thus after an initial analysis phase, testing of production wafers proceeds as usual. The algorithm only modifies acceptance ranges of conventional test data.