# STATISTICS FOR IMPROVEMENT OF I. C. PROCESS CONTROL

T. J. Kobylarz
F. H. Herman
Department of Electrical Engineering
Stevens Institute of Technology
Hoboken, New Jersey

A. J. Graf
P. C. Calella
Picatinny Arsenal
Dover, New Jersey

## SUMMARY

The use of test patterns is a valuable vehicle for monitoring production of large scale integrated circuit wafers with respect to the expected systems performance of the circuits. The role of such test patterns is to ascertain whether salient process control parameters are satisfied during the manufacture of a wafer. A questionable assumption is that the measurements, made at the location of the test patterns, are indicative of the process control parameters for the remainder of the wafer. One anticipates that a probabilistic validity of this assumption will vary inversely with the geometric distance between a test pattern and an integrated circuit chip.

This paper develops an algorithm, based on a collection of statistical data, which remedies the uniformity assumption of process control parameter measurements. It introduces the concept of a special "test" wafer as opposed to the "production" wafer, alluded to above. The test wafer consists solely of test patterns and is used to gather mean and variance data of the process parameters for the production runs. Because the process parameters are determined for an entire test wafer, one can statistically relate process parameter variation on the wafers.

Assume that the acceptance ranges for the parameters have been defined. By utilizing measurements of test patterns that are already present on production wafers, Bayesian analysis can be performed on the aforementioned statistical data. Consequently, a parameter distribution can be obtained which incorporates both the parameter measurements usually available and statistical information reflecting parameter non-uniformity. The above approach, together with an acceptance range for the parameter and a percentile confidence, enables a confidence interval to be established for the production wafer test pattern data. Usually, this confidence interval can be computed prior to testing subsequent production wafers. Thus after an initial test wafer analysis phase, testing of production wafers proceeds as usual. The algorithm only modifies acceptance ranges of conventional test data.

# I. INTRODUCTION

Recent efforts in improving integrated circuit reliability have led to more critical evaluation of the entire manufacturing process. One of the primary reasons for this increased concern in reliability is that more and more circuitry is being integrated into chips. Today large scale MOS memories, shift registers, and calculator systems are available as single chips. Soon computer subsystems will be available as unit devices. Increased lead count and circuit complexity have already made exhaustive testing of large scale integrated circuits (LSI) economically unfeasible.[1,2] It is also obvious that increased circuit complexity implies the need for increased reliability at the transistor level.

In the face of the growing problems brought on by larger integration, it has become increasingly important to control the manufacturing process at its many stages. Within the scope of existing process control, better design techniques can be incorporated which will "build-up" reliability.[3]

If the integrated circuit process technology is to be controlled, there must exist means for monitoring the effect of the process parameters. More specifically, there must be some correlation possible between measurable circuit parameters and the parameters of the fabrication process.[4] For example, diffusion characteristics control transistor characteristics such as gain and leakages. By measuring the electrical characteristics of a single transistor, it is possible to infer what the process parameters were which produced it. It must be realized that for a single wafer, the effects of the process vary over the wafer. If there are many transistors

on the wafer, the value of gain for the transistors will be distributed over some nominal range.

Techniques for the process control of silicon integrated circuit quality and reliability at the wafer level have been studied and implemented by many research institutes as well as integrated circuit manufacturers.[5-10] The control techniques vary from a single test transistor and capacitor on each chip to several test patterns on each wafer. These test sites are used to monitor and evaluate diffusion characteristics, wafer and oxide purities, mask alignments, product yield, product life, as well as unusual failure mechanisms which may occur due to stressed conditions.

To demonstrate the variations of testing procedures within the IC manufacturing field, several manufacturers were contacted. Among them were RCA and Solid State Scientific, Inc. The RCA testing procedure consists of five test patterns which are strategically placed on each wafer. Each test pattern consists of an NPN transistor, a PNP transistor, a capacitor, and a resistor. Among the measurements made on each test pattern are $V_{th}$, $I_D$ and $V_{DS}$ on the transistors, the capacitance of the capacitor, and the resistance of the resistor. Each pattern must fall between specified limits for the wafer to be accepted.

Solid State Scientific, on the other hand, places one test transistor and one capacitor on each chip to be tested randomly for $V_{th}$, $I_D$, $V_{DS}$, and capacitance. If these test patterns lie within fixed limits, the wafer is accepted.

These examples reflect the current approach to process monitoring. It is inherently assumed by these procedures that the test transistors and

capacitors represent the condition of the entire wafer on which they lie. The acceptable range of each parameter is supposed to reflect the range within which the circuit elements will operate acceptably in a circuit, and within which the failure mechanisms will be minimized. The way in which these parametric ranges are established is often through much experience with simple circuits or the circuit elements themselves. Extrapolation to complex circuit configurations is always questionable. To the degree that topological sensitivity analysis can be conducted, this extrapolation is often defendable. But it must be realized that even then, it is usually assumed that the parametric measurements on the test section of an integrated circuit are assumed to characterize the entire circuit physics.

The use of test transistors to monitor the above mentioned process parameters becomes less meaningful as the area of the integrated circuit "real-estate" increases. One cannot assume that these parameters will remain constant over the large area of LSI circuits. Only a few isolated test sites can be placed on a chip, and then only on the perimeter. Direct circuit probing is not feasible due to the relative size of probes compared to that of high-density circuit elements. Since they are not isolated, circuit elements cannot be individually tested. Thus, it is apparent that one cannot determine spatial parameter variations directly for an I. C.

## II. STATISTICAL APPROACH USING TEST WAFERS

In attempting to overcome the difficulty of accounting for significant parameter variation over the area of an I. C., it is natural to turn to a statistical approach. We wish to incorporate prior knowledge of spatial parameter variation with the information acquired by testing the few test sites on the production wafer. Using these two sources of information plus

the a priori knowledge of the acceptable range for the parameters, we wish to obtain an improved decision rule for accepting or rejecting the wafer. It is assumed that circuit element models and the particular circuit topology provide sufficient information for direct determination of this acceptable parameter range.[11]

Since prior knowledge of the parameter variation is required for the proposed approach, let us first consider of what this knowledge is to consist and how such information can be practically acquired. In a sense, one can assume that the parameters are independent so that each may be considered separately. We will also assume that a single test pattern is sufficient to perform the electrical measurements required for determining the parameter value at the site of the test point. Furthermore, regard the test pattern to be sufficient for evaluating all parameters of interest. These requirements are stated in the interest of simplifying the presentation of what follows. An extension to a more general case will be discussed later.

Let us now consider the source of variation of a process parameter. The variation will occur at two primary levels. Since control over the process is not perfect, the parameter will vary from run to run. The "nominal" or average value for a particular wafer reflects the value for the "run" or "heat" in which it was produced. The second source of variation is the variation of the parameter over a given wafer. This spread corresponds to a variance with respect to a mean. The variance will be assumed statistically independent to the mean value and known. The way in which this value can be determined will be considered shortly.

Our prior statistical knowledge can be specified as follows. On any wafer, the parameter is considered to be normally (Gaussian-normal) distributed with unknown mean and known variance. The mean, which is a random variable with respect to a run, can also be regarded as normally distributed with known mean and variance. The choice of normal distributions enable closed form solutions of the mathematics that follows. It is also a natural choice from the fact that continuously distributed variables are often normal. Non-normal distributions are considered briefly in the concluding sections.

In order to determine a distribution for the mean, we consider a special "test" wafer as illustrated by Figure 1.

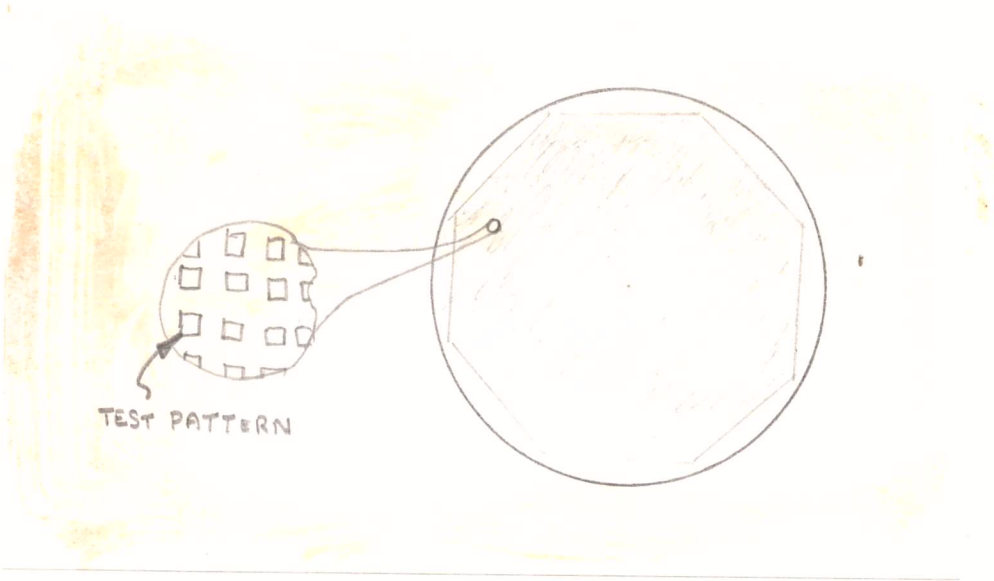


Figure 1. Test wafer.

This wafer is made up entirely of test pattern sites. Each site is a test pattern appropriate for making electrical measurements relating to the parameter value at that point. The sites also include the necessary probe lands. By testing all test sites, the mean and variance for each test wafer can thus be determined. A large number of these test wafers are initially produced in many different runs. They may be randomly scheduled along with the regular production wafers. Once these wafers have been produced and tested, the distribution for the parameter mean can be determined. Using the average parameter values of each test wafer, a mean and variance is computed, and these two values then determine the distribution of the wafer mean, $\mu_w$. This distribution was determined for test wafers only, but it is assumed that the process parameter will be distributed over a wafer according to statistics which are independent of the type of wafer. This follows from the fact that the test wafers and the production wafers are manufactured in common runs. Thus, the distribution of the parameter mean is assumed to correspond to both types of wafer. We determine the distribution using test wafers, but we will use it for the production wafers.

The wafer variance, that is the variance of the parameter on a given wafer, is also determined from the data gathered on the test wafers. The sample variance for each test wafer is computed, and then the average of these values is used as the wafer variance, $\sigma_w^2$. This value is thus an expected value. As previously stated, the wafer variance is assumed to be constant for each wafer, whether it be a test wafer or a production wafer.

It should be pointed out that the distribution of the mean is assumed time-invariant. Also, there is an assumption that the parameter spatial

variation is not correlated with the spatial position on the wafer. That is, knowledge of the relative or absolute spatial position of a point on a wafer does not introduce any significant information as to what the parameter value will be. When this is not an appropriate assumption, and a specific correlation does exist, it should be taken into account. For instance, if the perimeter of a wafer tends to have lower parameter values, one may choose to avoid placing chips near the perimeter and also not have test patterns in this region. The period during which the initial data is gathered on the test wafers corresponds to a learning period. During this period, one can also observe whether the assumption of normally distributed random variables and lack of spatial correlation are really valid. One can also determine if a constant variance is a valid assumption.

The prior knowledge of parameter variation has now been specified. In the next section, we consider how to incorporate this information in a statistically based testing procedure.

## III MATHEMATICAL ANALYSIS

It would be useful to know the parameter probability distribution for each production wafer. Using this distribution it would be possible to establish a decision rule on accepting or rejecting the wafer relative to an acceptable range for the parameter. Since this distribution is unknown in practical situations, we wish to consider how the information obtained via the test wafers can be combined with the information available from measuring the limited number of test sites on the production wafer.

Let us now review the previous statistical formulation in a precise manner. It is assumed that the parameter in question exhibits a normal distribution with known variance, $\sigma_w^2$ and unknown mean $\mu_w$. The mean is also assumed to be a random variable with known mean $\mu_m$ and variance $\sigma_m^2$. It has been previously stated how $\mu_m$, $\sigma_m^2$, and $\sigma_w^2$ are obtained. These statistics apply to both the test wafers and the production wafers.

At each of N test sites on a production wafer, the parameter X may be evaluated resulting in the N values $x_1, x_2, \ldots, x_n$. A Bayesian approach will be used to obtain a revised distribution for the mean, $\mu_w$ conditional on the N measurements on the production wafer. Then this revised distribution will be employed to obtain the distribution of the parameter on the particular test wafer being examined.

The first step may be obtained from Breipohl's paper[12] on Kalman filtering. It must be assumed that the measurements at the test sites may be regarded as independent events characterized by the parameter distribution. If the distance between test sites is large compared to the diameter of the test site, and if no significant spatial correlation exists between test points, this may be reasonable assumption. (During the learning period in which test wafers are used, the existence of high correlation to spatial position can be determined.)

Restating Breipohl's results in our notation, the Bayesian revised distribution is found to be normal with mean

$$\mu_{m,N} = \frac{\sigma_m^2 \sum_{i=1}^{N} x_i + \mu_m \sigma_w^2}{\sigma_w^2 + N\sigma_m^2} \qquad (1)$$

and variance

$$\sigma_{m,N}^2 = \frac{\sigma_m^2 \sigma_w^2}{\sigma_w^2 + N\sigma_m^2} \quad (2)$$

where the second subscript denotes the revised estimate conditional on N observations. We immediately observe that

$$\lim_{N\to\infty} \mu_{m,N} = \sum_{i=1}^{N} x_i / N \quad (3)$$

which is the sample mean, and that

$$\lim_{N\to\infty} \sigma_{m,N}^2 = 0 \quad (4)$$

The results of (3) and (4) are expected since as the number of observations on the product wafer grows large, the sample approaches the population.

It is now possible to obtain an estimate of the distribution for the process parameter. The parameter distribution was specified in terms of a known variance, but an unknown mean, and it was assumed normal. The density function can be considered as a conditional probability density function. It is conditional since it depends on the value of the mean, where this mean is in turn specified through an absolute distribution. Let the random variable $\mu_w$ correspond to the mean, and let the random variable Y correspond to the parameter value at some point on the production wafer. Let the following density functions be defined that characterize the conditional situation. From the

above discussion, we write the revised distribution for the wafer mean as

$$f_{\mu_w}(\theta) = \frac{1}{\sqrt{2\pi}\,\sigma_{m,N}} \exp\left\{-\frac{(\theta-\mu_{m,N})^2}{2\sigma_{m,N}^2}\right\}$$

where it is obvious that (5)

$$p\{\mu_w \le \theta_1\} = \int_{-\infty}^{\theta_1} f_{\mu_w}(\theta)\, d\theta .$$

The density function for the parameter distribution, conditional on the wafer mean value is

$$f_{y|\mu_m}(y|\theta) = \frac{1}{\sqrt{2\pi}\,\sigma_w} \exp\left\{\frac{(y-\theta)^2}{2\sigma_w^2}\right\}. \quad (6)$$

To determine the absolute density function for a parameter measurement, one integrates the product of (5) and (6) as

$$f_y(y) = \int_{-\infty}^{\infty} f_{y|\mu_m}(y|\theta)\cdot f_{\mu_m}(\theta)\, d\theta. \quad (7).$$

Substituting (5) and (6) into (7), one obtains

$$f_y(y) = \int_{-\infty}^{\infty} \frac{1}{2\pi\,\sigma_{m,N}\,\sigma_w} \exp\left\{-\frac{1}{2}\left[\frac{(y-\theta)^2}{\sigma_w^2} + \frac{(\theta-\mu_{m,N})^2}{\sigma_{m,N}^2}\right]\right\} d\theta. \quad (8)$$

If the terms of the exponential are expanded, put over a common denominator, then collected as coefficients of $\theta^2$, $\theta^1$, and $\theta^0$, and finally normalized with respect to $\theta^2$, the exponential expression can be written as

$$\exp\left\{-\frac{1}{2}\left[\frac{\theta^2 - 2\theta\left(\frac{\mu_{m,N}\sigma_w^2 + y\sigma_{m,N}^2}{\sigma_w^2+\sigma_{m,N}^2}\right) + \left(\frac{y^2\sigma_{m,N}^2 + \sigma_w^2\mu_{m,N}^2}{\sigma_w^2+\sigma_{m,N}^2}\right)}{\left(\frac{\sigma_w^2\sigma_{m,N}^2}{\sigma_w^2+\sigma_{m,N}^2}\right)}\right]\right\}$$

It would be helpful to obtain a normal form with respect to the variable of integration. $\theta$, since then the integration could be easily done. To obtain such a form, one must complete the square of the quadratic in $\theta$. Doing this, the exponential expression becomes

$$\exp\left\{-\frac{1}{2}\left[\frac{\theta - \left(\frac{\mu_{m,N}\sigma_w^2 + y\sigma_{m,N}^2}{\sigma_w^2+\sigma_{m,N}^2}\right)}{\frac{\sigma_w^2\sigma_{m,N}^2}{\sigma_w^2+\sigma_{m,N}^2}}\right]^2 - \frac{1}{2}\frac{(y-\mu_{m,N})^2}{\sigma_w^2+\sigma_{m,N}^2}\right\} \quad (9)$$

We are now in a position to write the integral in a standard form. The second expression in the exponent as given by equation(9) can be moved outside the integral due to the property of exponentials, since it is constant with respect to the variable of integration. Equation (8) can now be written as

$$f_y(y) = \frac{\exp\left[\frac{-(y-\mu_{m,N})^2}{2(\sigma_w^2+\sigma_{m,N}^2)}\right]}{\sqrt{2\pi(\sigma_w^2+\sigma_{m,N}^2}} \cdot$$

(mult by next exponential)

is accepted. If the level falls between these two thresholds, additional testing is carried out. The process stops when either no more test sites are available (rejection), or when absolute acceptance or rejection has occurred. The selection of the two thresholds and the number of test sites probed at each step of the sequence will be heuristic at best.

## IV. IMPLEMENTING STATISTICAL PROCESS CONTROL

It would be very difficult to define an absolute program for implementing the methods discussed so far. This is true because decision on various phases of process control must be based on complex information. Often, the experience of the process control engineer cannot be established in a well organized format. Nevertheless, a simple adaptation of the above techniques will be described in order to illustrate the fundamental features of our statistical approach.

Figure 2 shows how the production of an integrated circuit might utilize a statistical approach for process control. After the circuit is designed, sensitivity analysis is performed in order to determine the range of values for each parameter which suggests satisfactory circuit performance. In general, these ranges may be interrelated so that one must consider the acceptable range as a multidimensional surface. It will be assumed that the parameters may be considered separately in order to simplify the discussion.

The next step involves the circuit topology. Since a parameter range must be satisfied at many locations on the integrated circuit, the event of an acceptable parametric distribution represents the intersection of many simultaneous events. For instance, suppose the circuit contains ten

$$\int_{-\infty}^{\infty} \frac{1}{\sqrt{2\pi}\,\sigma_w \sigma_{m,N}} \Big/ \sqrt{\sigma_w^2+\sigma_{m,N}^2}\; \exp\left\{-\frac{1}{2}\cdot \frac{\left[\theta-\left(\mu_{m,N}\sigma_w^2+y\,\sigma_{m,N}^2\right)\right]^2}{\frac{\sigma_w^2\sigma_{m,N}^2}{\sigma_w^2+\sigma_{m,N}^2}}\right\} d\theta$$

The integral is in Guassian-normal form and is equal to one. We therefore obtain

$$f_y(y) = \frac{1}{\sqrt{2\pi(\sigma_w^2+\sigma_{m,N}^2}} \cdot \exp\left\{-\frac{1}{2}\cdot\frac{(y-\mu_{m,N})^2}{(\sigma_w^2+\sigma_{m,N}^2)}\right\} \quad (10)$$

which is also of the Guassian-normal form. The distribution for the process parameter Y is therefore normal with the mean given by equation (1) and variance given by

$$\sigma_y^2 = \sigma_w^2 + \sigma_{M,N}^2 . \quad (11)$$

The effect of the uncertainty of the wafer mean is to increase the a priori variance by the variance of the mean distribution. From (2), it is again clear that as the number of test sites on the production wafer is increased, the variance corresponding to the distribution of the process parameter on this

wafer approaches the a priori variance. For this reason, one may choose to use the sample variance computed using the test data of this wafer for $\sigma_w^2$ rather than the average value previously mentioned. The choice can be made after observing the results of the test wafers. When the variance is not consistent from wafer to wafer, the sample variance becomes the better choice.

The problem of using the distribution of a process parameter to define an acceptance decision rule is still not entirely resolved, at this point. If only a single location of the I. C. chip was affected by the parameter, one would simply determine the area under the density function curve over the interval of the acceptable range and compare the resultant probability to a threshold value. If the density function area was greater than this threshold, the wafer would be acceptable and if less than this value, rejection would occur. Even the decision on the threshold would be a complex task involving many economic factors. When one can identify a discrete number of wafer areas sensitive to the parameter, on the chip, one can raise the probability corresponding to the acceptable range to the power equal to this number, thus implying independent Bernoulli trials. When a discrete number of such areas cannot be identified, one must resort to some soul-searching to "pick" a confidence level.

Finally it is possible to define a sequential testing procedure[13] using the above techniques. We have previously assumed that all test sites on a production wafer are probed. One may instead probe only a fraction of these sites providing selection is randomized. Two thresholds must be defined. If the probability level corresponding to the parameter range of acceptance is less than the smaller threshold, the wafer is immediately rejected. If this probability level is above the higher threshold, the wafer

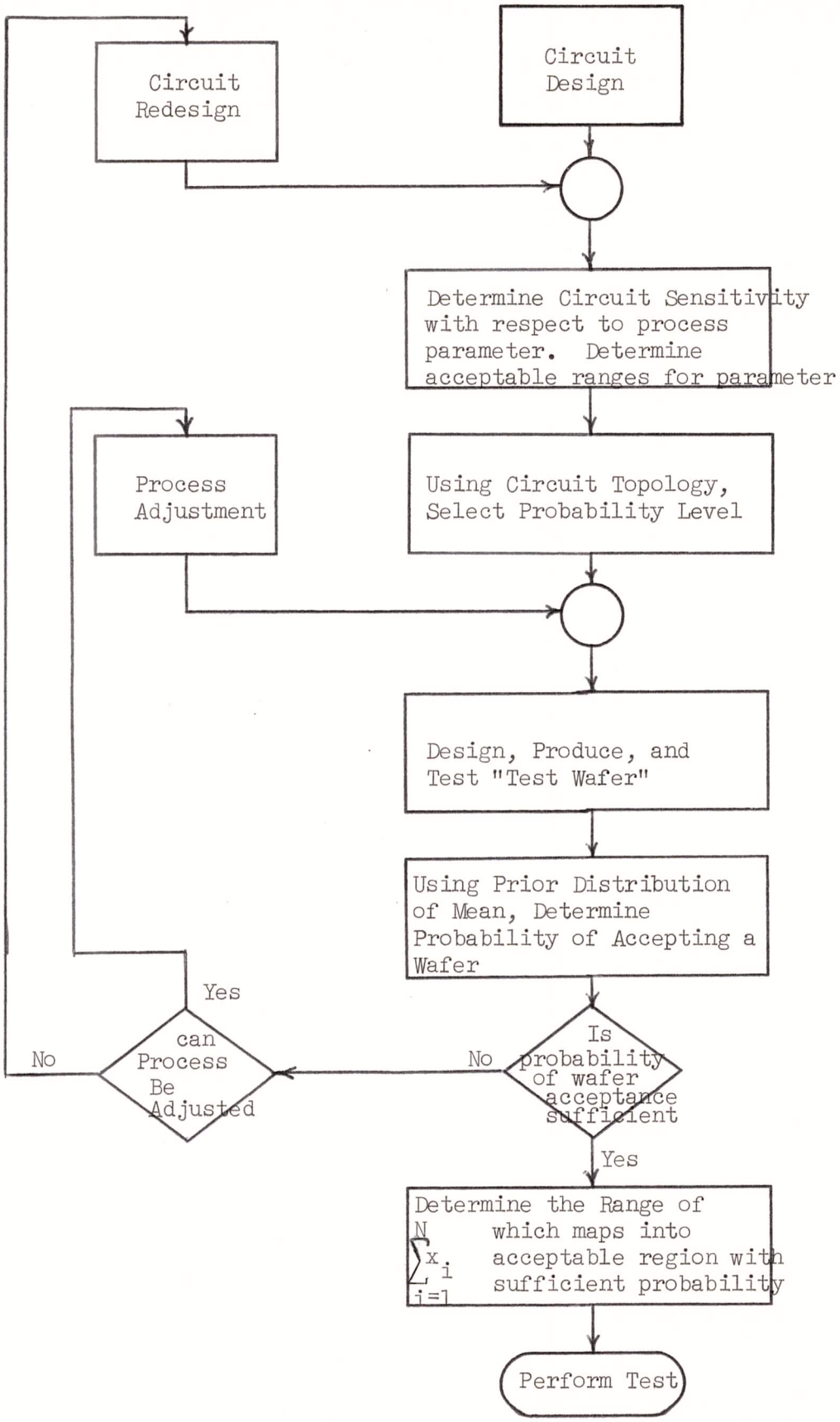


Figure 2 Implementing Statistical Process Control

transistors. If the parameter value for each one can be considered an independent event, then the probability of all of them having an acceptable value is equal to the probability of a random transistor having an acceptable value, raised to the tenth power. Often it is not possible to represent the circuit in terms of a discrete number of independent events. Parameter effects are not usually contained in discrete locations, nor is the effect at one location absolutely independent of the effect at another. Thus the power that one might raise the probability of a single event is a subjective number. We shall assume that the confidence level can be selected, and is known a priori.

Once the process parameter ranges have been selected, test wafers are produced under the process conditions of production wafers. The test wafers are made entirely of primative test patterns normally found on the production wafer. After a sufficient number of these have been produced and tested for parameter values, the distribution of the mean value of the wafers and the average wafer variance can be computed as previously described.

This prior distribution can be used to provide an indication of the level of wafer acceptance. Using equations (1), (2), and (10) by letting $N = 0$, (i.e. prior to product wafer test), the distribution for the parameter on the production wafer is normal with mean $\mu_m$ and variance equal to the sum of $\sigma_w^2$ plus $\sigma_m^2$. Using this distribution, one can compute the probability corresponding to the acceptable parameter range and the topology determined exponents described previously. This probability can be regarded as the prior probability that a production wafer will be acceptable. A decision must be made as to whether this acceptance level is desirable. If the indication rejection rate due to the parameter is unreasonable, then

either the process must be adjusted or the circuit must be redesigned to allow for less sensitivity to the parameter variation. Again, this decision is subjective.

Once the prior acceptance rate is deemed usable, the testing of production wafers can proceed. If the number of measurements on a production wafer is fixed, it is a simple matter to determine the range of value for the sum of these measurements that leads to acceptance of a wafer. This may be verified by observing that only equation (1) requires the values of the measurements. The determination of the acceptable range of the measurements can be accomplished prior to production wafer testing. Thus the only computation required during the production acceptance testing is summation of the test results, and then threshold comparisons. Even if the number of tests, N, can vary, threshold values corresponding to each N can be determined. Thus once the initial steps of the flowchart of Figure 2 are obtained, acceptance testing of wafers using the statistical approach is very simple.

It should be pointed out that all testing, whether on test wafers or production wafers, should be preceded by visual inspection. Cosmetic defects are removed by neglecting the affected area, whether it be test transistor or chip. This is one reason for computing separate thresholds for different values of N. On a production wafer, a chip having a cosmetic defect should be "scratched" and its test transistors not used for parameter screening. Justification of this follows from the fact that visual inspection can normally occur prior to chip testing and because the event of a cosmetic defect can be considered independent of parameter variation statistics.

## E. NON-NORMAL DISTRIBUTIONS

Let us consider briefly how the above techniques apply to the situation in which either the parameter distribution, or the mean distribution, is non-normal. In this situation, the use of the test wafer to gather a prior distribution for the mean is still appropriate. The major difference lies in the computational procedure. Since generally the integration required for the Bayesian analysis and for the evaluation of equation (7) do not yield closed-form solutions, numerical integration must be used. Since both such computations require the data from the production wafers, it is clear that prior determination of the confidence interval for a parameter is not possible as in the Normal case. The computations involving the Bayesian analysis and equation (7) must be done after the test patterns on a production wafer are probed. This requires a computer to be on-line with the wafer inspection station. Either a time-sharing terminal or a dedicated mini-computer can perform the necessary requirements.

## CONCLUSIONS

The statistical approach to process control as outlined in this paper allows one to consider the effects of process parameter variations for production wafers. Only statistical approaches appear feasible since direct monitoring of this variation is presently beyond the state-of-the-art for complex, large scale integrated circuits. By the use of test wafers, it is possible to obtain an estimate of the distribution of the effective parameter values. Bayesian analysis allows this estimate to reflect the dynamics of the data obtained from a limited number of parameter measurements on the production wafer.

When the wafer mean corresponding to a parameter and the parameter itself have normal distributions, closed form solutions are obtainable for the parameter distribution on the production wafer. Because of this, much of the algorithm computations can be carried through prior to actual testing of the production wafer. This allows for easy implementation of process control related to monitoring process parameter variations.

Lack of a normal distribution usually results in great difficulty for finding closed form solutions to the Bayesian revision of the mean distribution and/or the final estimate of the parameter distribution. In this case, the mathematics is similar, but the solution must be obtained numerically. Thus computation must be repeated for each production wafer, making implementation of the statistical techniques dependent upon on-line computer capability.

When the parameters cannot be considered separately, the approach becomes complex. Such a situation arises when the acceptable ranges for the parameters are dependent. The distribution estimation based on the testing procedure is as before, assuming that the parameter values themselves are independent random variables. What does change is the decision step in which the probability of acceptable parameter values is computed. If the decision function is a linear function of the parametric value, this function is a linear combination of independent random variables. Then the distribution of the decision function involves a convolution of the distributions of all the parameters. If all the parameters are normally distributed, the convolution can be simply evaluated without direct computation.[14]

The major problem may occur in evaluating the decision function. The acceptability region may be specified as several inequalities. Linear programming techniques or pattern recognition theory can be used in this situation. When the decision surface is nonlinear, both the determination of the decision function and the distribution of this function must be obtained by more complex techniques not considered here.

REFERENCES


1. Runyon, S. (1972) "Focus on MSI/LSI Testors." Electronic Design, Vol. 20, No.17. pp 60-69.
2. Salvador, J. (1972) "The Realities of Testing Digital I. C!s." Electronic Products Magazine, June 19, 1972. pp 65-68.
3. vanBeek, H. W. (1972) "MOS/LSI Circuit Design:Designing-in Reliability," 10th Annual Proceedings, Reliability Physics, sponsored by IEEE, pp 36-41.
4. Schroen, W. H., Aiken, J. G., and Brown, G. A. (1972) "Reliability Improvement by Process Control," 10th Annual Proceedings, Reliability Physics, sponsored by IEEE, pp 42-48.
5. Baron, F. J. and Myers, C. F. "Toward Making LSI Work", Motorola Monitor, 6, No. 3.
6. Miller, F., Test Sites for Microelectronics, No. 7/4, pp 1-10, Paper presented at the 1969 Western Electronic Show, San Francisco, Calif. August 20-21, 1969.
7. Herr, E. A., "Techniques for the Control of Integrated Circuit Quality and Reliability," G.E. Semiconductor Prod. Dept., Syracuse, N. Y. Report No. IR-8-232.
8. Anon. "Manufacturing in-Process Control and Measuring Techniques for Integrated Circuits", Westinghouse Elec. Corp. Molecular Electronics Div., Elkridge, Md., Rept. No. IR-8-140 (II)
9. Schlegel, E. S., "Study of Failure Modes of Multilevel Large Scale Integrated Circuits," Philco-Ford, Corp., Microelectronics Div., Blue Bell, Penna., Rept. No .NASA-CR-99100
10. Herr, et al, "The TEG - A Test Element for the Control of Quality and Reliability of Integrated Circuits" General Electric Technical Information Series Rept No. R 68EGP1.

11. Herskowitz, G. J. (1968) Computer-Aided Integrated Circuit Design, McGraw-Hill, New York.

12. Breiphl, A. M. (1969) "Kalman Filtering and Its Application to Reliability," IEEE Trans. Reliability, Vol R-18, No. 3, pp 127-130, August 1969.

13. Mood, A. M. and Graybill, F. A. (1963) Introduction to the Theory of Statistics, McGraw-Hill, New York.

14. Herman, F. H. and Kobylarz, T. J., "Bounds on Linear Combinations of Independent Random Variables." Submitted for publication.